said vertical walls and conductive polysilicon of said one of the conductivity types deposited into said trenches to define a polysilicon gate; a source region of said one conductivity type formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; a drain contact connected to said substrate; whereby said MOSFET has a reduced on resistance.

C2 Contd

9. (Amended) A power MOSFET having reduced on resistance comprising, in combination; a P type conductivity substrate; an epitaxially deposited N type layer of the other conductivity type deposited atop said P type substrate [and] to form an epitaxial layer having a substantially constant concentration throughout its volume; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; a P type concentration source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; and a drain contact connected to said substrate.

C3

C4

11. (Amended) The MOSFET of claim 10 wherein said epitaxial [region] layer has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

Please add the following new claims:

C5 Contd

--16. (New) A method for producing a trench MOSFET structure comprising:

forming an epitaxial layer of a first conductivity type on a substrate of a second conductivity type;

forming at least one trench in said epitaxial layer;

forming an insulative layer on walls of said at least one trench;

introducing polycrystalline silicon of said second conductivity type into said at least one trench;

forming an insulative layer covering said at least one trench; and

forming a source region of said second conductivity type in said epitaxial layer.

17. (New) A method of producing a trench MOSFET structure according to claim 16, further including forming highly doped contact regions in said epitaxial layer.

18. (New) A method of producing a trench MOSFET structure according to claim 16, further including forming a source contact on said source region.

19. (New) A method of producing a trench MOSFET structure according to claim 17, further including forming a source contact on said source region.

20. (New) A trench-type power MOSFET according to claim 1, further having a highly doped contact regions at a top portion of said vertical invertible channel.

21. (New) A power MOSFET according to claim 4, further comprising highly doped contact regions in said epitaxial layer.

22. (New) A power MOSFET having reduced on resistance according to claim 9, further comprising highly doped contact regions in said epitaxial layer.--

IN THE DRAWINGS:

Please amend Fig. 2 as shown in red on the attached copy thereof.

REMARKS

Claims 1-15 are in the application. All claims are rejected. Claims 14 and 15 are canceled. Claims 1, 4, 9 and 11 are amended. New claims 16-22 are added. No new matter is added.

DRAWINGS

Applicant submitted, on March 27, 2000, a preliminary Amendment containing